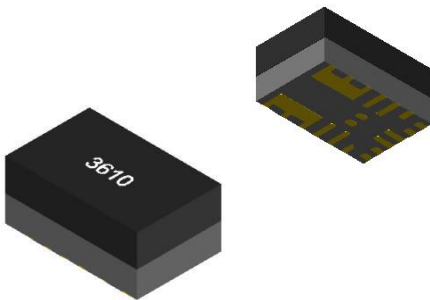


## 4.5~18V Input, 1.2A Output, DC-DC Ceramic Substrate Adjustable Buck Module



### 1 Features

- 1.2A output current
- Wide input voltage range: 4.5V-18V
- Output Voltage: 0.6V-5.5V
- Switching Frequency: 1MHz
- Efficiency up to 95%
- Soft Start
- Small size, surface mount package: LGA (5mm×3.2mm×2.2mm)

### 2 Applications

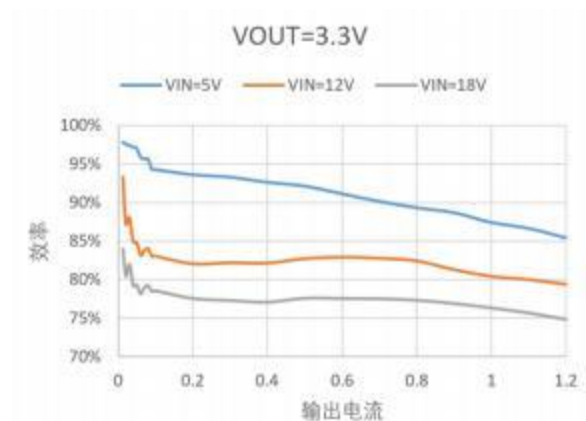
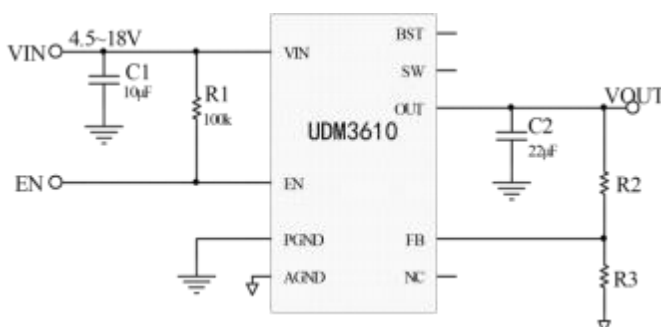
- Industrial control
- Medical imaging equipment
- Telecommunications and network applications
- Alternative to linear regulators (LDO)
- Miniaturized applications

### 3 Description

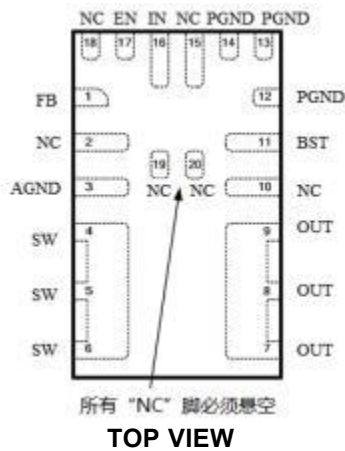
The UDM3610 is a DC-DC buck power module with synchronous rectification control. It integrates an inductor, power MOSFETs, and filtering capacitors. The UDM3610 provides a complete power solution, requiring only a few external passive components to achieve a wide input voltage range of 4.5V to 18V, a rated output current of 1.2A, adjustable output voltage, and excellent load and line regulation.

The UDM3610 features comprehensive protection functions, including overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), and overtemperature protection (OTP). The UDM3610 minimizes the use of external components and is packaged in an LGA-20 (5mm × 3.2mm × 2.2mm) package.

### Typical Application Circuit



## Pin Configuration



Pin	Symbol	Description
1	FB	Output voltage adjustment pin; connect a resistor with a precision of 1% or better to GND
2,10,15, 18,19,20	NC	No connection required; leave floating
3	GND	Analog ground. Internally connected to PGND; no external connection to PGND is required.
4,5,6	SW	Switching output. Lay out large copper areas on pins 4, 5, and 6 to enhance heat dissipation
7,8,9	V <sub>OUT</sub>	Module voltage output pin; connect directly to the positive terminal of the load. An external output filter capacitor must be connected to PGND.
11	BST	Bootstrap pin. The module internally integrates a bootstrap capacitor; no external connection is required, leave floating.
12,13,14	PGND	Power ground. Reference ground for the module's input and output voltages. Special attention should be paid to PCB design. It is best to use copper pour and via designs.
16	VIN	Input voltage positive terminal. Provides power input to the internal power and control circuits. Operating voltage range is 4.5V to 18V. Low ESR and ESL capacitors should be used for decoupling and filtering, and the capacitors should be placed as close as possible to the module's VIN pin, using wide traces and multiple vias where possible.
17	EN	Enable pin. Connecting the pin to a high logic level enables the module, while grounding the pin disables the module output. The pin must not be left floating.

## Ordering Information

Product Model	Input		Output	Dimensions and Package	Packaging
	Input Range	Nominal Input			
UDM3610	4.5V~18V	--	0.6V~	5mm×3.2mm×2.2mm (LGA)	Packaged in a box

## Electrical Characteristics

Absolute Maximum Ratings	Conditions	Minimum Value	Nominal Value	Maximum Value	Units
$V_{IN}, EN$		-0.3		20	V
$V_{SW}$		-0.3		20	V
VFB Pin Voltage		-0.3		6	V
BST Pin Voltage		-0.3		23	V
$V_{OUT}$		-0.3		6	V
Storage Temperature		-65		+150	°C
Reflow Soldering Temperature				+245	°C
Electrical characteristics	Conditions	Minimum Value	Nominal Value	Maximum Value	Units
Input Voltage Range		4.2		18	V
Input Undervoltage Lockout threshold (Rising)		4.0	4.3	4.5	V
Input Undervoltage Lockout Threshold (Falling)		3.6	3.8	4.0	V
Minimum Start-Up Voltage		4.5			V
Quiescent current	$V_{EN}=2V, V_{FB}=V_{REF} \times 105\%$		350		μA
Shutdown current	$V_{IN}=12V, V_{EN}=0$		5	10	μA
Switching Frequency			1000		KHz
Efficiency	$V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A$		84		%
EN Threshold (Rising)		1.0	1.1	1.2	V
EN Threshold (Falling)		0.85	0.94	1.05	V
EN Input Current	$V_{EN}=2V$	2.3	2.5	2.7	μA
Maximum Duty Cycle			80		%
Minimum On-Time			80		ns
Soft-Start Time			0.8		ms
FB voltage		0.588	0.6	0.612	V
Line regulation	$V_{OUT}=3.3V, 5V < V_{IN} < 18V, I_{LOAD}=1.2A$			±0.5	%
Load regulation	$V_{IN}=12V, V_{OUT}=3.3V, 0A < I_{LOAD} \leq 1.2A$			±1.6	%
Ripple and noise	$V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=1.2A, C_{out}=22\mu F, \text{Bandwidth: } 20MHz$		30		mV
Dynamic load response	50-100% $I_{LOAD}, di/dt=2A/\mu S, C_{out}=22\mu F$		480		mV

## Electrical Characteristics(continued)

Structural Characteristics	Conditions	Minimum Value	Nominal Value	Maximum Value	Units
Dimensions	5mm×3.2mm×2.2mm				mm
Weight			1.5		g
Environmental Adaptability	Conditions	Minimum Value	Nominal Value	Maximum Value	Units
Operating temperature (junction temperature)		-40		125	°C
High-Temperature Storage (Ambient Temperature)	+125°C , 48h			125	°C
High-Temperature Operation (Ambient Temperature)	+85°C , 24h; Low Input Voltage, Nominal Input Voltage, High Input Voltage, 8 hours each; $V_{IN}=60V$ , $V_{OUT}=12V$ , $I_{OUT}=2.4A$			85	°C
Low-Temperature Storage (Ambient Temperature)	-55°C , 24h	-55			°C
Low-Temperature Operation (Ambient Temperature)	-40°C , 24h; Low Input Voltage, Nominal Input Voltage, High Input Voltage, 8 hours each	-40			°C
Humid Heat	High-Temperature and High-Humidity Stage: 60°C , 95%;  Low-Temperature and High-Humidity Stage: 30°C , 95%;  10 cycles of 24h each	30		60	°C
Temperature Shock	High Temperature: 125°C,  Low Temperature: -55°C,  High and low temperatures of one hour each for a cycle, a total of 32 cycles of testing	-55		125	°C

Note 1: Stress above the values listed in the "Absolute Maximum Ratings" section may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect the reliability and lifespan of the device.

Note 2: The maximum continuous output current may be derated due to the junction temperature of the FHT4623.

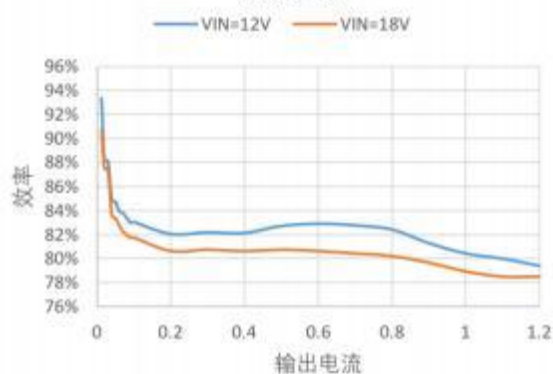
Note 3: The performance specifications of the UDM3610 are guaranteed over the entire internal operating stability range of -40°C to 125°C. Note that the maximum internal temperature is determined by specific operating conditions, PCB layout, the package's rated thermal resistance, and other environmental factors.

## Typical characteristics

Unless otherwise noted, test conditions are  $V_{IN}=12V$ ,  $V_{OUT}=3.3V$ ,  $T_A=25^{\circ}C$ .

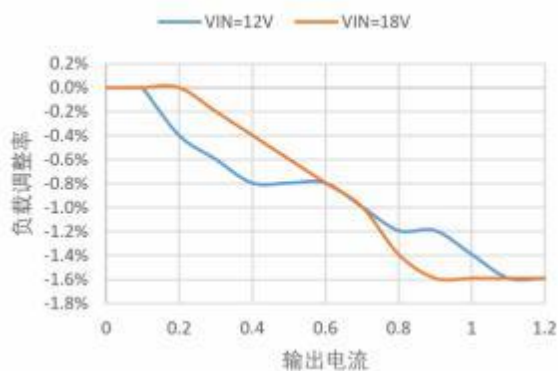
### Efficiency

$V_{OUT}=5V$



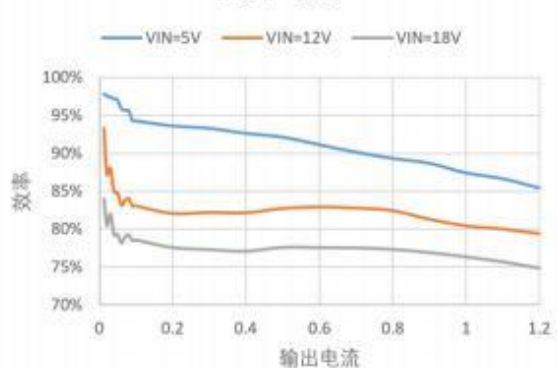
### Load regulation

$V_{OUT}=5V$



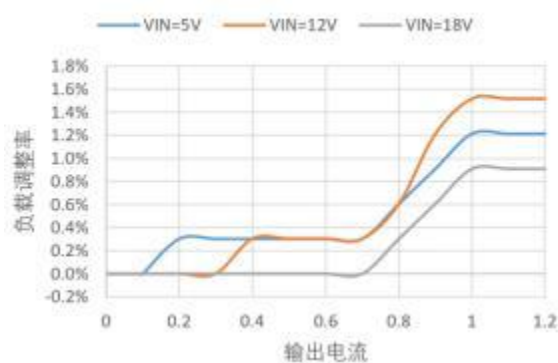
### Efficiency

$V_{OUT}=3.3V$



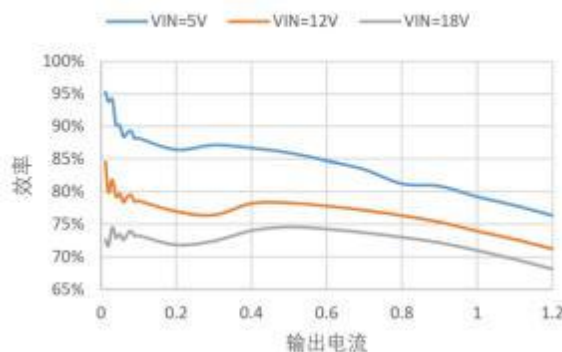
### Load regulation

$V_{OUT}=3.3V$



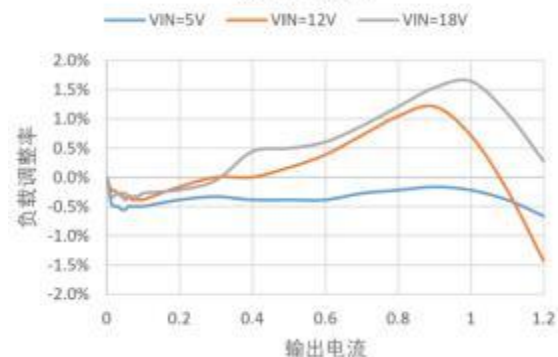
### Efficiency

$V_{OUT}=1.8V$



### Load regulation

$V_{OUT}=1.8V$



## Operation

### summary

The UDM3610 is a DC/DC buck power module with synchronous rectification control. It integrates an inductor, power MOSFETs, and filtering capacitors. The UDM3610 provides a complete power solution, requiring only a few external passive components to achieve a wide input voltage range of 4.5V to 18V, a rated output current of 1.2A, adjustable output voltage, and excellent load and line regulation.

The UDM3610 features comprehensive protection functions, including overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), and overtemperature protection (OTP). The UDM3610 minimizes the use of external components and is packaged in an LGA-20 (5mm × 3.2mm × 2mm) package.

### Internal Soft-Start (SS)

The soft-start function is designed to prevent overvoltage at the output during the startup process. The UDM3610 has an integrated soft-start feature: when the module starts, its internal circuit generates a ramp-up voltage (SS) from 0V to 0.6V. When the SS voltage is below the internal reference voltage VREF (0.6V), the internal error amplifier uses the SS voltage as the reference voltage. When the SS voltage exceeds the internal reference voltage, VREF is used as the reference voltage again. The soft-start time for SS is internally set, with a typical value of 0.8ms.

### Startup and Shutdown

If both VIN and VEN exceed their respective thresholds, the module starts. The internal reference voltage circuit starts first, generating a stable reference voltage, followed by the enabling of the internal regulator. The regulator provides a stable power supply to the rest of the circuit. There are three conditions that can cause the chip to shut down: VIN is too low, VEN is too low, and overtemperature shutdown protection. During the shutdown process, the signal loop is first blocked to prevent accidental triggering. Subsequently, the COMP voltage and internal power supply are pulled down. The open-drain output is not affected by this shutdown command.

### Overcurrent Protection and Short Circuit (OCP)

The UDM3610 features cycle-by-cycle current limiting protection. When the peak inductor current exceeds the internal peak current limit threshold, the upper switch turns off, and the lower switch remains on until the inductor current drops below the internal valley current limit threshold. The valley current limit circuit reduces the operating frequency (after the peak current limit threshold is triggered). At the same time, the output voltage continues to drop until VFB falls below the undervoltage (UV) threshold (typically 42%). Once the UV threshold is triggered, the UDM3610 enters hiccup protection mode, periodically restarting the module. This protection mode is particularly useful in the event of an output short to ground, significantly reducing the average short-circuit current, mitigating thermal issues, and protecting the module. Once the overcurrent condition is resolved, the UDM3610 exits the hiccup protection mode.

### Overtemperature Shutdown Protection (OTP)

To prevent damage from overheating, the UDM3610 stops switching when the internal chip temperature exceeds 150 °C. Once the temperature falls below the threshold (typically 130 °C), the module resumes operation.

### Undervoltage Lockout Protection (UVLO)

Undervoltage Lockout protection (UVLO) ensures that the module stops operating when the input voltage is insufficient. The UVLO comparator in the UDM3610 monitors the output voltage of the internal LDO (VCC). The typical rising threshold for UVLO is 4.3 V, while the typical falling threshold is 3.85 V.

### Error Amplifier (EA)

The UDM3610 uses a dynamic transconductance amplifier as the error amplifier (OTA). The error amplifier compares the FB voltage with the internal 0.6V reference voltage (VREF) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP voltage, which is used to control the current in the power MOSFETs. The optimized internal compensation network minimizes the number of external components required, greatly simplifying the design of the control loop.

## Application information

### Output voltage setting

The module's output voltage can be set by connecting pull-up and pull-down resistors between VOUT and GND at the FB pin. The reference calculation formula is as follows:

The output voltage is set by an external resistor divider. (Refer to the typical application on the front page.) First, select R1, and then calculate R2 using equation (1):

$$R2 = \frac{R1}{\frac{VOUT}{0.6V} - 1} \quad (1)$$

Figure 1 and Table 1 provide recommended parameters for common output voltages in the feedback network.

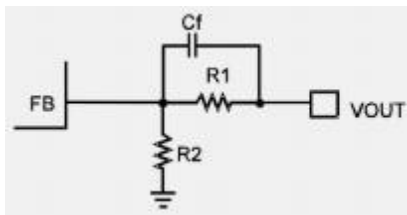


Figure 1 Feedback Network

Table 1 Recommended Parameters for Common Output Voltages

VOUT(V)	R1(kΩ)	R2(kΩ)	Cf(pF)
5	39	5.36	33
3.3	39	8.66	33
2.5	39	12.4	33
1.8	39	19.6	33
1.5	39	26.1	33
1.2	39	39	33
1	39	59	33

Under normal circumstances, it is recommended to set the output voltage between 0.6V and 5.5V. However, the output voltage can be set higher than 5.5V. In such cases, due to larger inductor ripple currents, the output voltage ripple will be greater. An additional capacitor is needed to reduce the output voltage ripple.

If the output voltage is set higher, thermal management becomes more important. Refer to the "PCB Layout Guidelines" on this page for better thermal performance.



### Input Capacitor Selection

Since the input current to the buck module is discontinuous, it is necessary to design an input capacitor in the application. The input capacitor maintains the DC input voltage while also providing AC current. The input capacitor must have sufficient ripple current capability. The RMS current through the input capacitor can be estimated using equation (2):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

Using low ESR capacitors can provide better performance. In most cases, it is recommended to use ceramic capacitors with X5R or X7R dielectrics, with a capacitance of 10μF or higher. X5R and X7R type ceramic capacitors maintain stable performance over a wide range of temperatures and voltages, effectively reducing the ripple in the input voltage.

### Output Capacitor Selection

An output capacitor (C2) is required to maintain the DC output voltage. It is recommended to use ceramic, tantalum, or low ESR electrolytic capacitors. For optimal performance, it is suggested to use low ESR capacitors to reduce the output voltage ripple. The output voltage ripple can be estimated using equation (3):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (3)$$

Where  $f_s = 1000\text{kHz}$ ,  $L_1 = 1.5\mu\text{H}$ , and  $R_{ESR}$  is the equivalent series resistance (ESR) of the output capacitor.

### PCB Layout Guidelines

The UDM3610 highly integrates the components required for power conversion, eliminating most of the tricky issues related to PCB layout. However, it is still necessary to optimize the PCB routing as much as possible to ensure proper operation. Even with high integration, you need to ensure good grounding and thermal performance when using the module. The recommended layout is shown in Figure 4:



## Application information(continued)

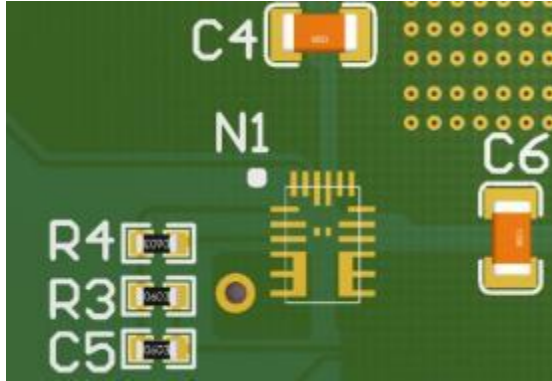


Figure 2 PCB Layout Diagram

1. Place the RFB resistors used for feedback voltage division as close as possible to their corresponding FB pins;
  2. Place the Cin capacitors as close as possible to the Vin and PGND connections of the UDM3610;
  3. Place the Cout capacitors as close as possible to the Vout and PGND connections of the UDM3610;
  4. Connect all PGND pins to the largest possible copper pour on the top layer, avoiding any breaks in the ground connection between external components and the UDM3610;
2. To achieve good thermal performance, use vias to connect the PGND copper pour area to the internal ground plane of the PCB, providing a good ground connection and a thermal path to the PCB plane. Since they are close to the internal power handling components, the UDM3610 can benefit from good thermal dissipation through these vias connected to the internal GND plane of the PCB. The optimal number of thermal vias depends on the design of the PCB. For example, if the PCB uses very small vias, more thermal vias may be needed to ensure adequate heat dissipation.

## Typical Application Circuit

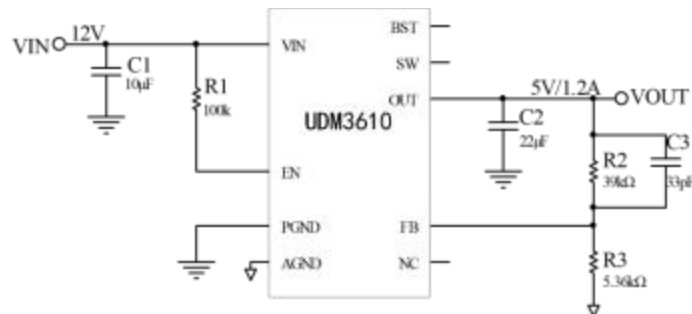


Figure3 VOUT=5V,IOUT=1.2A

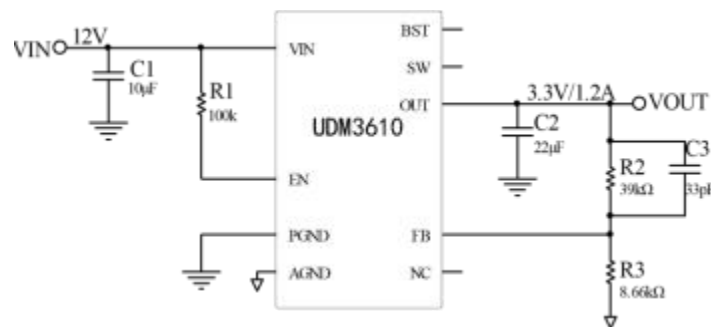


Figure4 VOUT=3.3V,IOUT=1.2A

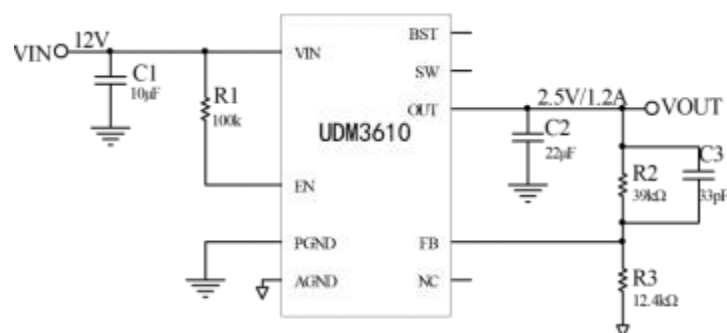


Figure5 VOUT=2.5V,IOUT=1.2A

## Typical Application Circuit(continued)

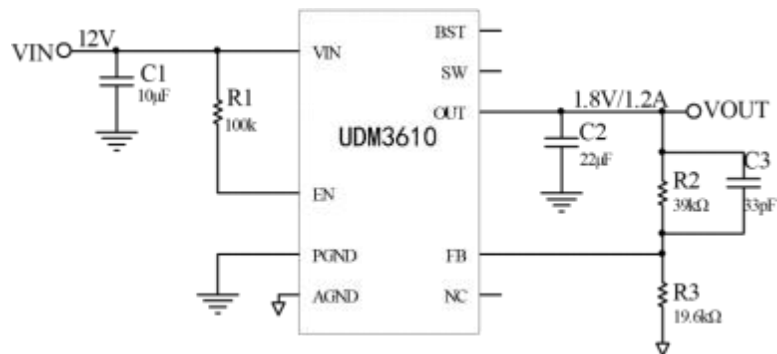


Figure6 VOUT=1.8V,IOOUT=1.2A

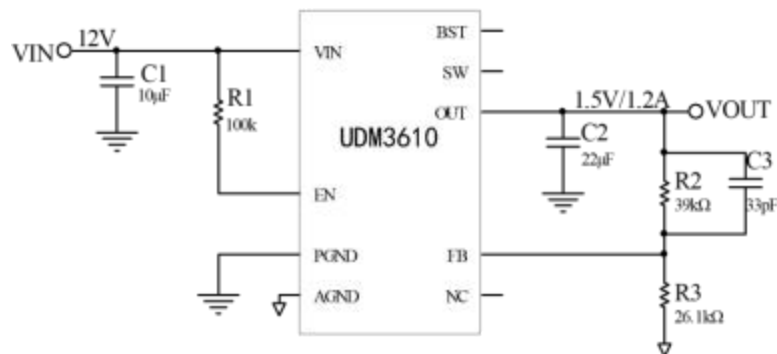
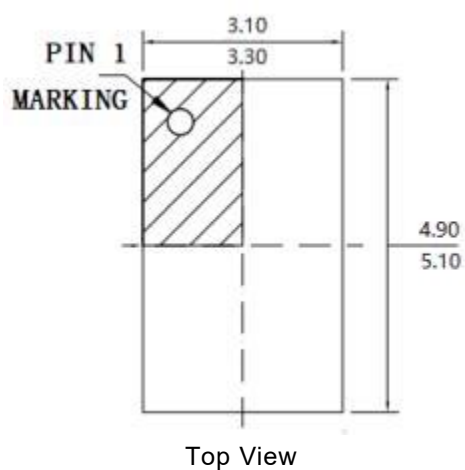


Figure7 VOUT=1.5V,IOOUT=1.2A

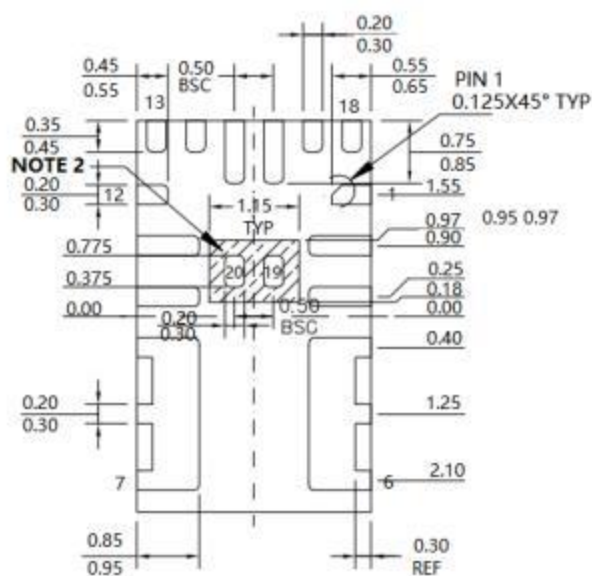
## Package Information

### LGA Package

20 Pins (5mm×3.2mm×2.2mm)



Top View



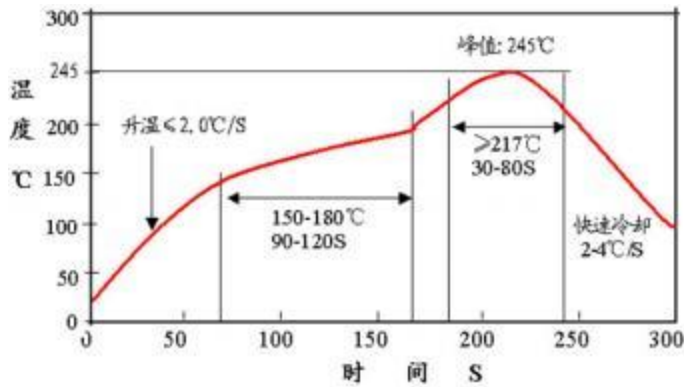
Bottom View



Side View

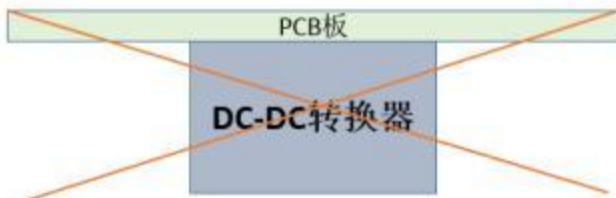
## Soldering and Storage Precautions

### Recommended Reflow Soldering Profile



### Note:

1. Due to the size of the module, do not place the module on the bottom side of the board for reflow soldering to avoid module drop.



2. For bulk and unpackaged products, store them in a dry box (the relative humidity in the dry box should be kept below 10%). For products that are still in their original packaging, store them in a dry box whenever possible.
3. Before mounting on the board, strictly follow the baking conditions to dry the samples: bake at  $125^\circ\text{C}$  for more than 48 hours, and control the reflow soldering temperature to within  $245^\circ$